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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
PORTKA, GARY J	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 12/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/612,849	AU ET AL.	
	Examiner	Art Unit	
	Gary J. Portka	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☒ Claim(s) *20-21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/5/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-21 are pending.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on March 5, 2004 was considered by the examiner.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-2 and 18-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Barlow et al., US 2004/0168019 A1 (hereinafter "Barlow").

5. As to claim 1, Barlow discloses an *integrated circuit memory device comprising a memory array* (vector register file 8) *having a page* (squares of Fig. 5) *of multiport memory cells that span at least X columns and Y rows, said page configured to support writing/reading of first data vectors to/from the X columns, and writing/reading of second data vectors to/from the Y rows, where X and Y are unequal integers* (see Abstract, Figs. 1 and 4-5, paras. 0035-0041, 0046-0049 and 0054-0056; X and Y may each be considered any unequal number of the memory cells, from 1 to 8, or alternatively, X and

Y are unequal integers when considering the recited page as two horizontally adjacent squares as shown in Fig. 6).

6. As to claim 2, *the first vectors and second vectors are Y-bit and X-bit words* respectively when considering the recited page as two horizontally adjacent squares as shown in Fig. 6.

7. As to claims 18-19, Barlow discloses *a method of operating a memory as a FIFO* (since it is used to stream data, para. 0002), *comprising writing a page* (square of Fig. 5) *by transferring a first plurality of FIFO data vectors into columns of a first cache* (14, Fig. 1, or more particularly 8, Fig. 4) *of the array, and copying the page from the first cache into embedded or external RAM* (connected at 4, Fig. 4) *by transferring a plurality of memory data vectors from rows of the cache* (see Abstract, Figs. 1 and 4-5, paras. 0035-0041, 0046-0049 and 0054-0056; vector register file 8 may be considered a cache since it is a high speed memory between the processor and the memory, and data may be written in one orientation, i.e., columns, and read from the other, i.e., rows, see paras. 0059 and 0071-0074).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Barlow.

10. Claims 4, 6, 8, and 10-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Barlow, in view of Braceras et al., US 5,561,781 (hereinafter "Braceras").

11. As to claims 4, 6, 8, and 10-12, the device of Barlow may be considered a FIFO since it is used to stream data (para. 0002). As to claims 4, 6, 8, and 10-12, Barlow teaches a three port device, but does not teach a quad-port device. However, Braceras teaches the use of a quad-port device, as depicted in Figs. 3 and 4 (it is noted that the CRB/SBB are not required to incorporate this teaching). It would have been clear to an artisan that the addition of a port to Barlow might make the device more costly, yet would likely have improved performance due to the parallel capabilities of more ports. Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to use a quad-port device, because more ports increases parallelism which improves performance.

12. As to claims 3 and 13, Barlow does not specifically disclose that Y=72 and X=36. However, it is clear that this is an arbitrary choice by the Applicant and is not of importance to the inventive concept. In Barlow the memory is not constained to the sizes used, and thus an artisan would have recognized that the system is not constrained to particular values of X and Y, and that any values within reason could be selected therefor, in order to meet one's design parameters. Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to select Y=72 and X=36, because the values are not constrained and may be selected as desired.

13. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Barlow, in view of Blake et al., US 5,752,264 (hereinafter "Blake").

14. Claims 9 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Barlow, in view of Braceras, and further in view of Blake.

15. As to claims 5, 9, and 14, neither Barlow nor Braceras teach a check bit generation and error detection and correction circuit for the memory vectors. However, Blake teaches that it is advantageous to protect data in a cache, using ECC, and that a typical ECC implementation uses just such a circuit (col. 4 lines 43-55). Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to use check bit generation and error detection and correction circuitry as recited, because this was known means to avoid errors when storing data.

16. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Barlow, in view of Braceras, and further in view of McGehearty et al., US 6,446,157 (hereinafter "McGehearty").

17. As to claim 7, neither Barlow nor Braceras disclose switching between two caches. However, McGehearty teaches that operations are advantageously switched between two cache banks (the same as the recited two cache devices) to minimize delays while equalizing data in and out of the caches (see Abstract, col. 2 lines 35-45, and col. 3 lines 35-38). Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to switch between first and second caches, because this was known to minimize delays and equalize data in and out of the cache.

18. Claims 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Barlow, in view of Duh et al., US 6,795,360 B2 (hereinafter "Duh").

19. As to claims 15-17, Barlow substantially discloses the invention as described above with regard to claims 1 and 6. Barlow does not disclose the memory is written to and read from via different width busses. However, Duh teaches that in FIFO memories it is beneficial to provide a device that is flexibly matched to different bus widths, to allow matching busses of unequal sizes (see col. 3 lines 26-51). Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to write and read via different width busses as recited, because it was known to use such a device to match different width busses.

Allowable Subject Matter

20. Claims 20 and 21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

21. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

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5,148,523 DRAM with column/row vectors of different length (col. 3 lines 1-2).

22. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gary J. Portka whose telephone number is (571) 272-4211. The examiner can normally be reached on M-F 9:30 AM - 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Gary J Portka
Primary Examiner
Art Unit 2188

November 28, 2005

GARY PORTKA
PRIMARY EXAMINER